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| 10/629,049 | 07/28/2003 | Young-Joon Choi | 4591-343 | 5961 |

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| EXAMINER | |
|---|---|
| RAHMAN, FAHMIDA | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2116 | |

DATE MAILED: 11/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/629,049 | CHOI ET AL. | |
| | Examiner | Art Unit | |
| | Fahmida Rahman | 2116 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *28 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7-10 and 13-18* is/are rejected.

7)☒ Claim(s) *5,6,11 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/28/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-18 are pending.

### Information Disclosure Statement

The information disclosure statement (IDS) submitted on 7/28/2003 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

### Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy filed on 7/28/2003 has been received.

Should applicant desire to obtain the benefit of foreign priority under 35 U.S.C. 119(a)-(d) prior to declaration of an interference, a translation of the foreign application should be submitted under 37 CFR 1.55 in reply to this action.

### Drawings

Figure 1 should be designated by a legend such as "Prior Art", because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing

figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

## Specification

The disclosure is objected to because of the following informalities: line 34 of page 1 refers flash memory with the numeral 9. However, according to lines 33-34 of page 1, flash memory is represented by the numeral 4.

Appropriate correction is required.

## Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 14-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Gibson et al (US Patent 6601167).

For claim 14, Gibson et al teach a method for reading out data from a NAND flash memory (Fig 5 and Fig 6) in a computer system having a system controller (12 in Fig 1) and a buffer ("output data register" in line 10 of column 4), the method comprising:

- setting commands, addresses, and pages to be read out from the NAND flash memory (lines 24-30 of column 7);
- copying data of a first page from the NAND flash memory to the buffer (lines 8-11 in column 4);
- and copying data of a second page from the NAND flash memory to the buffer while transmitting the first page data from the buffer to the system controller (line 60 of column 3 through line 7 of column 4 mention that the system uses Gapless-read command, which eliminates inter-page latency outputs multiple pages sequentially. In addition, lines 61-64 of column 6 mention that the Gapless Read command pre-loads the first memory page into data register. Therefore, the second page must be copied from flash memory to the output register while it transmits the first page from output register to system controller) .

For claims 15 and 16, lines 60-63 of column 3 mention that the memory pages are output sequentially. In addition, lines 25-35 of column 7 mention that a non-volatile page resides in output data registers. Therefore, to output the pages sequentially, the system must copy the successive page into the output register while transmitting the previous page.

Claims 17-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Tang et al (US Patent Application Publication 2003/0206442).

For claim 17, Tang et al teach the following limitations:

A method for programming data from a NAND flash memory in a computer system (Fig 4) with a system controller and a buffer ([0007] in page 1), the method comprising:

- setting commands, addresses, and pages to be programmed to the NAND flash memory (Fig 4 shows the memory write operation. In addition, lines 21-25 of page 2 mention that the address translation unit facilitates writing data to memory. Thus, there is associated commands, addresses and data to be written in memory. Since, NAND flash memory supports sequential access, the memory is organized as pages. Thus, the data to be written has to be in the form of pages);
- successively loading data necessary for the pages to be programmed from the system controller to the buffer (lines 8-11 of [0023] mention that an interleave access mode may be employed if buffer region includes several buffering device. Thus, the system must load pages to the buffer successively);
- and sequentially programming the pages by using the data loaded to the buffer (lines 8-11 of [0023] mention that an interleave access mode may be

employed if buffer region includes several buffering device. Thus, the method comprises sequential program of the pages by using the data loaded to the buffer).

For claim 18, Tang et al support interleaved access of memory through buffer (lines 8-11 of [0023] of page 2). Thus, the data for one page has to be loaded into buffer while programming of one page continues.

**Claim Rejections - 35 USC § 103**

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant admission of prior art, in view of Kim (US Patent Application Publication 2003/0075609).

For claim 1, applicant admitted in pages 1-2 that the following limitations are cited in prior art:

A computer system (Fig 1) comprising:

- a system controller (1 in Fig 1) including a central processing unit (5 in Fig 1) and a memory bus controller(7 in Fig 1) and configured to operate in a first interface mode;
- a system memory (3 in Fig 1) connected with the system controller (1) through the system bus (2 in Fig 1);
- a NAND flash memory (4 in Fig 1) configured to store a system driving code ("boot code" in lines 32-33 of page 1 in specification; "BS" in 9 of Fig 1), an operating system program ("OS" in 9 of Fig 1), and user data for the computer system ("UD" in 9 of Fig 1);
- and an interface unit (8 in Fig 1) configured to communicate with the system controller through the system bus in the first interface mode (controller 8 is configured to communicate with 1 through 2) and configured to communicate with the NAND flash memory in a second interface mode (8 is configured to operate with 9).

However, the following limitations are not taught by the applicant's admitted prior art:

- the interface unit being synchronized with a clock signal generated in response to predetermined command information.

Kim teaches a system where the interface unit (120 in Fig 2) being synchronized with a clock signal (SCLK in Fig 3C) generated in response to predetermined command

information (Fig 3A shows that the clock SCLK is generated when the command line BS is free from BS0).

It would have been obvious to one ordinary skill in the art at the time the invention was made to combine the teachings of Kim and applicant's admission of prior art. One ordinary skill in the art would have been motivated to have a clock signal generated in response to predetermined command information, since it is not necessary to provide a continuous clock in the interface unit. The interface can be clocked only when it is accessed by the computer system (lines 13-15 of [0014] in page 1) and a significant power saving can be achieved by stopping the clock, since power consumption is related to clock speed.

For claim 2, Kim teaches a system wherein the interface unit (120 in Fig 2) comprises:

- a host interface unit (111) configured to communicate with the system controller through the system bus in the first interface mode (lines 1-2 of [0010] of page 1 mention that the interface with connected to host and transmits serial data. Thus, the interface unit operates with system controller through the system bus in the first interface mode);
- a register unit (112 in Fig 2) configured to store configuration information about the computer system, the NAND flash memory, and the command information (according to lines 6-8 of [0010] of page 1, the register 112 includes a command register, write register and read register. Since, flash

memory can store boot data, the read/write register can store configuration information about computer and the NAND flash memory. The command register stores command information);

- a buffer unit (113) for configured to store data of the NAND flash memory;
- an oscillator (117) configured to generate a clock signal to synchronize the interface unit ;
- a controller (115) synchronized with the clock signal and configured to control an inner operation of the interface unit in response to the command information (115 has to synchronize the data with the flash memory 110. Thus, it is configured to control the inner operation of the interface unit in response to command information); and
- a NAND flash interface unit (115 is interfacing with NAND flash memo0ry 110) synchronized with the clock signal and configured to communicate with the NAND flash memory via the controller in the second interface mode.

Kim does not teach the following limitations:

- Oscillator generates the clock signal in response to command information
- Controller is a state machine.

It would have been obvious to one ordinary skill in the art at the time the invention was made to modify the combined teachings of Kim and applicant's admission of prior art to generate the clock from oscillator in response to command information. One ordinary skill in the art would have been motivated to have a clock signal generated in response

to predetermined command information by putting AND gate with a select signal responsive to command information, since it is not necessary to provide a continuous clock in the interface unit. The interface can be clocked only when it is accessed by the computer system and a significant power saving can be achieved by preventing the clock, since power consumption is related to clock speed.

It would have been obvious to one ordinary skill in the art at the time the invention was made to modify the combined teachings of Kim and applicant's admission of prior art to build the controller with state machine, since state machine are widely popular in the art for their availability and ease of operation.

For claim 7, Kim teaches the computer system with following limitations:

The interface unit comprises:

- a first interface unit (111) configured to communicate with the system controller through the system bus in the first interface mode (lines 1-2 of [0010] of page 1 mention that the interface with connected to host and transmits serial data. Thus, the interface unit operates with system controller through the system bus in the first interface mode);
- a second interface unit (115) synchronized with the clock signal (Fig 3 shows that the system is synchronous with SCLK) and configured to communicate with the NAND flash memory in the second interface mode;

- a storage unit (116) configured to store information and data exchanged between the first and second interface units;
- and a control unit (117) synchronized with the clock signal and configured to control a transmission of the information and data between the first and second interface units.

For claim 8, 112 and 113 in Fig 2 of Kim are the register unit and buffer unit.

Claims 3 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant admission of prior art, in view of Kim (US Patent Application Publication 2003/0075609), further in view of Gibson et al (US Patent 6601167).

Applicant's admission of prior art, as modified by Kim do not teach that the interface unit comprises a power up detector to apply a power-sensing signal.

Gibson et al teach a system comprising power up detector (30) to generate power good signal as shown in Fig 6.

It would have been obvious to one ordinary skill in the art at the time the invention was made to combine the teachings of applicant's admission of prior art, Kim and Gibson et al. One ordinary skill in the art would have been motivated to include power up detector, since boot data within flash memory should be loaded when the power supply

generates proper operating voltages. The power up detector ensures that the power supply reaches appropriate voltage, which in turn ensures safe loading of boot code.

Claims 4 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant admission of prior art, in view of Kim (US Patent Application Publication 2003/0075609), further in view of Tang et al (US Patent Application Publication 2003/0206442).

Applicant's admission of prior art, as modified by Kim do not teach that the interface unit comprises an error correcting code synchronized with the clock signal and configured to perform an error test and correction of data of the NAND flash memory.

Tang et al teach the error correction code unit (340).

It would have been obvious to one ordinary skill in the art at the time the invention was made to combine the teachings of applicant's admission of prior art, Kim and Tang et al. One ordinary skill in the art would have been motivated to include error correcting code unit, since error correcting code will correct any reading errors to increase reliability (lines 7-9 of [0025] of page 3).

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over applicant admission of prior art, in view of Gibson et al (US Patent 6601167).

For claim 13, applicant admits that the following limitations exist in prior art:

A booting method for a computer system with a NAND flash memory (lines 30-35 of page 1 of applicant's disclosure) comprising:

- copying a system bootstrap code from the NAND flash memory in response to a power applying detecting state (line 31 of page 1 of applicant's disclosure mention that the NAND memory is the booting memory. Thus, the bootstrap code must be loaded from NAND flash memory in response to power applying detecting state);
- initializing the computer system according to the system bootstrap code (lines 1-10 of page 2 of applicant's disclosure mention that the system booting is performed by using NAND flash memory is the booting memory) ;
- copying an operating system code to a programmable memory from the NAND flash memory (lines 8-10 of page 2 of applicant's disclosure mention that the OS in moved from NAND memory to system memory);
- and executing the operating system code (lines 9-10 of page 2 of applicant's disclosure mention that OS is moved to system memory to perform the

system booting. Thus, the OS code is executed to complete the booting process)

However, applicant's prior art does not mention about copying the bootstrap code to the buffer and initializing the computer from the code stored in buffer.

The teachings of Gibson et al mention that the processors have prefetch buffer ahead of actual use of instructions by the processor (lines 45-50 of column 4). The boot code is stored there before processed by the processor.

It would have been obvious to one ordinary skill in the art to provide the prefetch buffer as mentioned by Gibson et al, since executing instructions from prefetch buffer increases the instruction execution efficiency.

**Allowable Subject Matter**

Claims 5-6 and 11-12 would be allowable if rewritten to include all of the limitations of the base claim and any intervening claims.

**Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fahmida Rahman whose telephone number is 571-272-8159. The examiner can normally be reached on Monday through Friday 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Fahmida Rahman
Examiner
Art Unit 2116

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